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FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/324,823
Filing Date	June 2. 1999
First Named Inventor	Takeshi Ide et al.
Examiner Name	Aung Soe Moe
Art Unit	2685
Attorney Docket No.	075834.00036

METHOD OF PAYMENT *(check all that apply)*

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1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		x =
Independent Claims		-3** =		x =
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	$500.00
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1601	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

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SUBMITTED BY

(Complete *(if applicable)*)

Name (Print/Type)	Robert J. Depke	Registration No. (Attorney/Agent)	37,607	Telephone	312-277-2600
Signature				Date	1/29/07

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TOTAL PAGES (Including Cover Page) 31 DATE: 1/29/07

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NOTES:

Inventor:	Takeshi Ide et al.
Serial No. :	09/324,823
Art Unit:	2685
Filed:	June 2, 1999
Attorney Ref.:	075834.00036

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TRANSMITTAL FORM

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Total Number of Pages in This Submission:

Application Number	09/324,623
Filing Date	June 2, 1999
First Named Inventor	Takeshi Ide et al.
Art Unit	2685
Examiner Name	Aung Soe Moe
Attorney Docket Number	075834.00036

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [x] Amendment/Reply
  - [x] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
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- [ ] Petition to Convert to a Provisional Application
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- [x] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
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Appeal Brief

Remarks

The Commissioner is hereby authorized to charge any fees due or to credit any overpayment to Deposit Account No. 50-3891.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Rockey, Depke, Lyons & Kitzinger 233 S. Wacker Drive, Chicago, IL 60606
Signature	
Printed name	Robert J. Depke
Date	1/29/07 Reg. No. 37,607

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	09/324,823	**Confirmation No.:**	2056
Applicant:	Takeshi Ide et al.		
Filed:	June 2, 1999		
TC/A.U.:	2618		
Examiner:	Aung Soe Moe		
Docket No.:	075834.00036		
Customer No.:	33448		

APPEAL BRIEF

I. REAL PARTY IN INTEREST

The real party in interest is Sony Corporation as a result of transfer of all right, title and interest to the subject matter of this Application Serial No. 09/324,823 via the Assignment recorded in the Patent Office in Reel 010170 Frame 0509 on August 16, 1999.

II. RELATED APPEALS AND INTERFERENCES

Applicants note that this case was first submitted to a Pre-Appeal Brief Request for Review on November 16, 2006. A decision was mailed on December 29, 2006. Applicants and the undersigned are unaware of any further related judicial proceedings, appeals, or interferences in relation to the instant Appeal.

III. STATUS OF CLAIMS

The claims currently stand in condition as modified by the Amendment of August 13, 2003 amending claims 1 – 3 and adding new claims 4 - 6, as further modified by the

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Amendment accompanying RCE of May 25, 2004, adding new claims 7 - 18, as further modified by the Amendment of January 10, 2005 amending claims 4 – 6 and canceling claims 7 – 18, and as finally modified by the Amendment of August 4, 2005 amending claims 1 – 3.

IV. STATUS OF AMENDMENTS

No Amendment After Final effecting the claims has been filed or entered by the Examiner. Accordingly, all remaining claims stand in the same condition as they did at the time of the August 4, 2005 Amendment to the Claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a solid-state image sensor device having an image sensing portion for performing photoelectric conversion and being able to operate in both progressive mode and in interlaced field mode. More particularly, the present invention is concerned with a technique for actively controlling a bias voltage applied to a substrate of the image sensing portion in order to ensure that a saturation signal quantity output from the device is substantially the same in both the interlaced field scanning mode, where adjacent pixels are mixed, and the progressive scanning mode, where adjacent pixels are not mixed.

As noted on page 1 of the specification, in recent years, solid-state image sensor devices being able to read-out image data in both a progressive scan mode and an interlaced scan mode have begun to appear on the market.

As clearly shown in Figure 2(B), during interlaced field reading, all of the pixels are read out, and vertically adjacent pixels are combined together. For example, during even

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field read-out, vertically adjacent pixels 4A and 3A are mixed together and transferred vertically as one data point. Similarly, vertically adjacent pixels 4B and 3B are mixed together in the second vertical CCD, and are transferred as one data point.

In contrast to interlaced field read-out, progressive read-out transfers all of the image signals accumulated in each of the photo sensing devices (1A – 4A and 1B – 4 B) independently and separately via the vertical CCD registers 4. (See page 1, line 15 – page 2, line 9).

As noted in the first full paragraph of page 2 of the specification, conventional solid-state image sensor devices implementing both progressive scan and interlaced field scan readout modes had the problem that a saturation signal quantity during progressive scan read-out becomes one half of that saturation signal quantity during interlaced scan read-out period. This was due to the fact that during interlaced field read-out, the accumulated charge of two image sensors are combined, such that double the quantity of charge is transferred via the Vertical CCD during interlaced field scan as compared to progressive scan. (See page 2, lines 19 – 24 which defines 'saturation signal quantity' as "The saturation signal quantity means a maximum signal quantity when a solid state image sensor device outputs a right signal..." and page 12, lines 10 – 15, which states that the "saturation signal quantity" is measured and compared after image read-out and mixing of adjacent charges for interlaced mode.)

Because of this relationship between the two scanning modes, and the fact that a single vertical CCD register had to support both modes, dynamic range of the image degraded during progressive mode read-out compared to interlaced field mode read-out.

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Applicant's invention is directed to a resolving this outstanding problem and providing an optimal balance between interlaced field mode read-out and progressive mode read-out.

More specifically, the present invention is directed to an imaging device employing a photodiode, preferably a Hole Accumulation Diode, and striking an optimal balance between interlaced field mode read-out and progressive mode read-out. As shown in Figure 1 and described on page 7, lines 11 through 24, the present invention requires a substrate bias generation circuit 7 which applies a substrate bias via a substrate terminal 2e to the imaging device as shown in Figure 3A as a function of whether the device is operating and interlaced field mode or progressive mode.

As noted on page 12, lines 10 – 13 and 19 - 23 of the specification, the quantity of the difference between the two voltages applied to the substrate in the progressive scan mode and the interlaced field scan mode is set beforehand so that the saturation signal quantity in the progressive scan mode will be substantially equivalent to that in the interlaced field scan mode after read-out of accumulated signals and mixing of charges in interlaced field mode read-out.

Applicants submit that the claims of the instant invention are directed to a novel method of overcoming the shortcomings and deficiencies of the prior art by applying different substrate bias voltages such that saturation signal quantities in both progressive and interlaced field mode are made substantially equivalent after image read-out. The prior art fails to teach or suggest such a device. Consistent with the forgoing, the independent claims of the instant application require the following:

Claim 1 requires a solid-state image sensor device 1 (See Fig. 1) having an image sensing portion 2 performing photoelectric conversion in both progressive mode in which all

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picture element signals are output independently, and interlaced mode in which interlaced scannings are performed and the picture element signals obtained in respective scannings in said image sensing portion are superimposed (See page 1, line 15 – page 2, line 9), said sensor device comprising: a photodiode 3 within the image sensing portion; and a substrate-bias generation circuit 7 (See Fig. 1 and page 9, lines 14 - 22) for applying a bias voltage ØSUB to the substrate of said image sensing portion (See page 11, lines 4 – 7) and for controlling said bias voltage in said progressive mode to be smaller than the bias voltage while operating in the interlaced mode (See page 4, lines 1 – 5 and page 12, lines 1 - 18); and wherein the applied bias voltages are chosen such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode (See page 12, lines 10 – 13 and 19 – 22).

Claim 2 requires a driving method for a solid-state image sensor device 1 (See Fig. 1) having an image sensing portion 2 including a photodiode 3 within the image sensing portion for performing photoelectric conversion said image sensing portion operating in both progressive mode in which all picture element signals are output independently, and interlaced mode in which a plurality of scannings are performed and picture element signals obtained in respective scannings are superimposed (See page 1, line 15 – page 2, line 9), said method including applying a bias voltage ØSUB to the substrate of said image sensing portion (See page 11, lines 4 – 7), wherein during said progressive mode said bias voltage is smaller than that in said interlaced mode (See page 4, lines 1 – 5 and page 12, lines 1 - 18); and wherein the applied bias voltages are chosen such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode (See page 12, lines 10 – 13 and 19 – 22).

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Claim 3 requires a camera comprised of a solid-state image sensor device 1 (See Fig. 1) having an image sensing portion 2 for performing photoelectric conversion and a substrate-bias generation circuit 7 (See Fig. 1 and page 9, lines 14 - 22), an optical system receiving incident light from a subject and forming an image on said image sensing portion of said solid-state image sensor device, a driving system for driving said solid-state image sensor device, and a signal processing system for processing the signal output from said solid-state image sensor device to obtain a video signal, wherein the image sensing portion includes a photodiode structure, and further wherein said driving system selectively operates in progressive mode in which all picture element signals are output independently, and interlaced mode in which a plurality of scannings are performed and the picture element signals obtained in respective scannings are superimpose (See page 1, line 15 – page 2, line 9), and wherein the bias voltage applied to the substrate in said progressive mode is smaller than that in said interlaced mode (See page 4, lines 1 – 5 and page 12, lines 1 - 18); and wherein the applied bias voltages are chosen such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode (See page 12, lines 10 – 13 and 19 – 22).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether the teachings of the *Yamaguchi* (U.S. Patent No. 6,342,921) reference in view of *Suzuki* (U.S. Patent No. 6,515,703) and *Suga* (U.S. Patent No. 4,963,980) provide the requisite teaching or suggestion in order to render obvious claims 1 – 2 under 35 U.S.C. §103(a).

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B. Whether the teachings of the *Yamaguchi* (U.S. Patent No. 6,342,921) reference in view of *Suzuki* (U.S. Patent No. 6,515,703), *Suga* (U.S. Patent No. 4,963,980), and *Lee* (U.S. Patent No. 5,904,493) provide the requisite teaching or suggestion in order to render obvious claims 4 and 5 under 35 U.S.C. §103(a).

C. Whether the teachings of the *Chang* (U.S. Patent No. 5,264,939) reference in view of *Suzuki* (U.S. Patent No. 6,515,703), and *Suga* (U.S. Patent No. 4,963,980) provide the requisite teaching or suggestion in order to render obvious claims 1 - 3 under 35 U.S.C. §103(a).

D. Whether the teachings of the *Chang* (U.S. Patent No. 5,264,939) reference in view of *Suzuki* (U.S. Patent No. 6,515,703), *Suga* (U.S. Patent No. 4,963,980), and *Lee* (U.S. Patent No. 5,904,493) provide the requisite teaching or suggestion in order to render obviated claims 4 and 5 under 35 U.S.C. §103(a).

VII. ARGUMENT

Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to obviate Applicant's presently claimed invention. As detailed below, the rejections set forth by the Examiner are improper.

A. The Cited *Yamaguchi*, *Suzuki*, and *Suga* References Fail to Obviate the Claimed Invention as specified in Claims 1 – 6.

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Applicants respectfully request reconsideration of the Examiner's rejection of claims 1 – 3 under 35 U.S.C. §103(a). Examiner has alternately rejected these claims in view of the cited prior art references of *Yamaguchi* (U.S. Patent No. 6,342,921), *Suzuki* (U.S. Patent No. 6,515,703) and *Suga* (U.S. Patent No. 4,963,980).

Under § 2143 of the MPEP, in order to establish a prima facie case of obviousness, the Examiner must meet three basic criteria. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." *MPEP §2143 rev. 3* (August, 2005). Applicants' assert that the Examiner has failed to establish a prima facie case of obviousness for at least the reasons that the prior art references fail to teach or suggest all of the claim limitations. Neither the primary reference nor any secondary reference provides any indication that two pre-determined bias voltages are applied to the substrate as a function of whether the imaging device is operating in progressive or interlaced field scanning mode, "so that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode."

Applicants note that the Examiner has conceded that the primary *Yamaguchi* reference fails to show any application of a bias voltage to the substrate of the image sensing portion, and thus necessarily fails to teach or suggest anything regarding variation of an applied bias voltage. (See page 3, first full paragraph of the May 16, 2006 Office Action). Additionally, the Examiner has conceded that neither the *Yamaguchi* nor the *Suzuki* reference show that the bias voltages are chosen such that a saturation signal quantity in the progressive

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mode is substantially equivalent to that in the interlaced field mode. (See page 4, first full paragraph of the May 16, 2006 Office Action).

The only issue Applicants wish to bring to the attention of the Board in regard to the *Yamaguchi* and *Suzuki* references is the proper distinction between progressive mode read-out and interlaced mode read-out. Progressive mode read-out is a method of reading-out charges stored in all of the image sensing devices in the imaging array at the same time, and wherein there is no mixing between adjacent photo-diodes. (See Column 2, lines 60 – 62 of Suzuki, which describes this mode and dismisses it as too costly compared to interlaced mode). Progressive mode read-out is labeled full-frame read-out in the *Yamaguchi* reference. (emphasis added). See, for example, Column 5, lines 34 – 37 of *Yamaguchi*, which associates the terms "full-frame readout" and "progressive mode readout" to both mean that all image sensors are read-out at the same time without mixing.

In contrast to progressive mode, interlaced mode involves the read-out of less than all of the imaging devices in the imaging array at the same time. Interlaced mode has been implemented in two ways, frame-mode and field-mode. (Note that frame-mode is distinct from full-frame mode). In field mode interlaced scanning, adjacent pixels are read-out and mixed together in the vertical CCD register. (See Column 1, lines 36 – 40). In frame mode interlaced scanning, odd rows are read-out first, and then after the vertical CCD is done transferring the odd rows, the even row pixels are then read out.

Importantly, and counter to the Examiner's assertions throughout the last Office Action, the only reference cited by the Examiner that discloses a true progressive mode read-out is the *Yamaguchi* reference (directed to full-frame and thinning mode). Importantly, however, *Yamaguchi* fails to disclose, teach, or suggest a device capable of running in both

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interlaced mode and progressive (full-frame) mode, and actually teaches away from such a device. For example, *Yamaguchi* teaches the advantages of utilizing a thinning method instead of an interlaced mode read-out when only a subset of the entire imaging array is needed in Column 9, lines 55 – 65.

The remaining references cited by the Examiner, *Suzuki* and *Suga*, are both directed solely to interlace scanning. There is no disclosure at all in either of these references to progressive mode read-out, absent the casual mention in Column 2, line 67 – Column 3, line 2 of *Suzuki* that progressive mode read-out is too expensive and is not generally used. While the remaining references do compare field-mode interlaced scanning in which adjacent pixels are mixed in the Vertical CCD to frame-mode interlaced scanning in which only the odd pixels are read-out and transferred (un-mixed) before the even pixels are read-out and transferred (unmixed), neither reference contains any disclosure, teaching, or suggestion regarding utilizing progressive mode and interlaced mode read-out in the same device. For at least this reason, Applicants submit that the Examiner's practice of equating frame-mode interlaced read-out as disclosed in *Suzuki* and *Suga* with the claimed progressive mode (full-frame in *Yamaguchi*) read-out is inaccurate and un-supported by the references.

Furthermore, in light of the fact that *Yamaguchi* teaches away from interlaced scanning, Applicants submit that there can be no teaching or suggestion to combine the *Yamaguchi* with either one of the *Suzuki* or *Suga* references.

Applicants submit that, for at least these reasons, the Examiner's rejection cannot be sustained and should be reversed on Appeal.

Absent the above contention regarding the cited prior art references, the single remaining contention between Applicants and the Examiner is whether the *Suga* reference

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discloses the claim limitation requiring that two pre-determined bias voltages are applied to the substrate as a function of whether the imaging device is operating in progressive or interlaced scanning mode, "so that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode."

FIG. 6 of the accompanying drawings shows the switching circuit of an electronic still camera of the above stated kind arranged to permit a selection between the field mode and the frame mode. The illustration includes an adder 60; signals 62_1 and 62_2 produced from odd-number field picture elements (hereinafter referred to as ODD picture elements) and even-number field picture elements (hereinafter referred to as EVEN picture elements) respectively; change-over switches S1 and S2 which are provided for a selection between the field mode and the frame mode; field mode selecting contacts A1 and B1; frame mode selecting contacts A2 and B2; a terminal A3 which is provided for reading a field image; and terminals B3 and B4 which are provided for reading the odd- and even-number field portions of the frame image signal, respectively. When the moving contacts of the field mode/frame mode change-over switches S1 and S2 are on the side of the frame mode selecting contacts A2 and B2, the information of the ODD picture elements and that of the EVEN picture elements are serially read out from the reading terminals B3 and B4 for every field. In case that the moving contacts of the change-over switches S1 and S2 are on the side of the field mode selecting contacts A1 and B1, the information of the ODD picture elements and that of the EVEN picture elements are added together by the adder 60 and read out from the reading terminal A3 as a field image.

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In relying upon the *Suga* disclosure, the Examiner states in the May 16, 2006 Office Action that "*Suga* '980 teaches the use of bias voltage control circuit (i.e., see Fig. 10, the elements 35 and 37) for a solid-state image sensor (i.e., CCD 31 of Figs. 10 & 11A), and the applied bias voltages (i.e., noted the voltages Va and Vb as shown in Fig. 11B; see col. 6, lines 30+) are chosen (i.e., see Col. 7, lines 1 – 10) such that a saturation signal (i.e., noted the Vsat as shown in Fig. 11C) quantity in the progressive mode (i.e., Noted the Frame Mode used as a progressive mode as discussed in the combination of *Yamaguchi* '921 and *Suzuki* '703 as discussed above) is **substantially** equivalent to that in the interlaced mode (i.e., Noted the Field mode used as an interlaced mode as discussed in the combination of *Yamaguchi* '921 and *Suzuki* '703 above) (i.e., as shown in Figs. 11B and 11C that the saturation signal Vsat for the Frame Mode is ***substantially*** equivalent to that of the field mode; see Col. 7, lines 1 – 25 and col. 7, lines 65+; and Figs. 11A – 11C, 12 and 13 of *Suga* '980)." (Emphasis in original, see page 4, 2nd full paragraph – page 5, line 2).

First and foremost, and as noted earlier, Applicants respectfully refute the Examiner's characterization of *Suga* as disclosing anything regarding progressive mode read-out. Full-frame interlaced read-out is not equivalent to progressive mode read-out.

In any event, Applicants note that the Examiner has relied solely upon the drawings (Fig.'s 11(B) and 11(C) of *Suga*) in order to anticipate the claim limitation requiring substantially equal saturation signal quantities in both the interlaced and progressive modes. (See, for example, the right ¼ portion of Fig. 11(C), where the Vsat lines for Field and Frame converge at Vsat-Photo Diode). Assumedly, this is because, in contrast to Figure 11(C), the corresponding portion of the supporting *Suga* text which the Examiner relies upon merely discloses exactly what *Suzuki* discloses. More specifically, the text of *Suga* merely states that

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the drain voltage VOFD should be set "at a relatively low level in frame mode" and "at a relatively high level" in field mode. (See Column 7, lines 4 – 9). Accordingly, Applicants submit that the sole remaining issue between the Examiner and Applicant's can be further narrowed to the question regarding what the drawings alone (Fig's 11(B) and 11(C)) of *Suga* disclose in regard to Applicant's independent claims.

Applicants submit that the term "saturation signal quantity" has been clearly defined at the bottom of page 2 of Applicant's disclosure as "a maximum signal quantity when a solid-state image sensor device outputs a right signal." Additionally, the term is defined on page 12, lines 10 – 13 of Applicant's disclosure to be the saturation signal quantity after the read-out of the signal charge by the read-out gate 2b (See Fig. 3A). Accordingly, this term takes into account the maximum saturation signal quantity of at least the photo-diodes and the vertical-CCD 4, and may also take into account the horizontal-CCD 5 shown in Fig. 1. See, *Oakley, Inc. v. Sunglass Hut Int'l*, 316 F.3d 1331, 1341 (Fed. Cir., 2003), in which the court stated that "a patentee may be his or her own lexicographer by defining the claim terms." As shown in Fig. 11(C) of the *Suga* reference, the saturation signal quantity of various portions of the device must be considered, including the Vsat of each single photo-diode, the Vsat of the Vertical CCD, and the Vsat of two times the Vsat of the single diode which comes into play during interlaced field mode read-out when two adjacent rows are combined in the Vertical CCD (See page 2, lines 10 – 15 of Applicant's disclosure).

Accordingly, Applicant's submit that the independent claims of the instant invention require that a saturation signal quantity of the device (i.e., the maximum signal quantity output when the solid-state image sensor device outputs a right signal) be substantially the same in both the interlaced field mode and progressive mode scan-outs.

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Additionally, Applicants submit that this must be the case as their invention is directed to solving the problem existing in the art that the saturation signal quantity when combined in the vertical transfer register in the interlaced field mode is double that of the saturation signal quantity in the vertical transfer register in the progressive mode. Accordingly, Applicant's submit that the term 'saturation signal quantity' cannot be construed to merely mean the saturation signal quantity of an individual photo-diode in the imaging device. Rather, and consistent with Applicant's disclosure, Applicant's submit that the ordinary use of the term 'saturation signal quantity' when used in terms of progressive and interlaced field mode readout must be construed to mean the ultimate saturation signal quantity read-out from the imaging device. Applicants submit that this definition is consistent with the prior art references. See, for example, column 2, lines 38 – 63 of *Suzuki*, which notes that the problem in the prior art and being addressed is one regarding the decrease in dynamic range between signals read into the Vertical CCD during progressive mode, and signals read into the Vertical CCD and mixed during interlaced field mode.

Furthermore, Applicants note that while the claims do not specifically limit coverage to interlaced field mode (and would appear to cover interlaced frame mode), additional claim elements effectively limit the coverage of the claim to field mode. More specifically, if a device was to use both progressive mode read-out and interlaced frame-mode read-out, there would be no mixing of signals in the Vertical CCD and hence no need to adjust the saturation signal level by modifying the substrate-bias voltage level applied to the substrate between the two modes. Because the claims currently require that the voltage bias applied to the substrate be smaller in the progressive mode than in the interlaced mode, the claim effectively

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forestalls reading on any currently existing device implementing both progressive-mode read-out and interlaced frame mode read-out on the same device.

In light of the forgoing, Applicants submit that the limitation "saturation signal quantity" must be construed to mean at least that signal quantity existing in the Vertical CCD (mixed in interlaced field mode, and non-mixed in progressive mode) after pixel read-out. Applicants further submit that, consistent with Federal Circuit case law and with their own definition of the term set forth in the specification, 'saturation signal quantity' should be construed to mean that signal quantity which is finally read-out from the solid-state image sensor output portion 6 when a right signal is output, as shown in Fig. 1 of Applicant's disclosure and described on page 9 of the text.

Based on either of the above constructions, Applicant's submit that *Suga* fails to anticipate the currently claimed invention. More specifically, and consistent with Column 7, lines 3 – 7, Fig. 11(B) of *Suga* merely discloses that the voltage applied to the substrate VOFD should be 'relatively higher' during field mode read-out than during progressive mode read-out. Fig. 11(C), on the other hand, is solely focused on the Vsat of a single photo-diode. The fact that the saturation levels converge on the right hand side of the Figure is immaterial, and actually teaches away from, the Vsat of the signal finally read-out from the device (or the Vsat of the signal existing in the Vertical CCD) being substantially equivalent during both progressive and interlaced field mode read-out. Applicant's claim requires that the bias voltages applied to the substrate during progressive and interlaced mode read-out are set beforehand such that the saturation signal quantity read-out from the device in both the progressive and interlaced mode is substantially equivalent. (See page 12, third full paragraph of Applicant's disclosure). Fig. 11(C) of *Suga* fails to address the Vsat of the

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signals in the CCD after mixing or upon final output from the imaging device, and furthermore, clearly teaches away from such signals having substantially equivalent saturation quantities.

More specifically, it is important to note that at the point of the graph at which the Examiner relies upon in order to assert that the saturation signal quantity of both the field and frame interlaced modes is substantially equivalent (the right ¼ portion of Fig. 11(C) where the Field and Frame lines converge) merely represents the Vsat of a single photo-diode. (See the legend on the ordinate axis of the Figure, which shows Vsat photo-diode, Vsat VCCD, and Vsat 2x photo-diode). Clearly, in this portion of the cited Figure, once the saturated signal for the field photo-diode is combined with a vertically adjacent saturated photo-diode, the saturation signal level in the vertical CCD of the field mode read-out will exceed the saturation signal level in vertical CCD of the progressive mode read-out. Furthermore, Applicant's note that their entire invention is directed to the range in the left ¾ of the *Suga* reference, wherein the saturation signal quantity of the individual photo-diodes is actively modified based on the scan-mode by changing the bias voltage applied to the substrate in order to ensure that the signals, once mixed in interlaced field mode in the Vertical CCD and not mixed in progressive mode, have substantially equivalent saturation signal quantities.

In light of the foregoing, and the fact that the Examiner has failed to cite any portion of the *Suga* reference which anticipates the claim limitation requiring that the saturation signal quantities are substantially equivalent in both interlaced (mixing) and progressive (no-mixing), the Examiner has failed to assert a prima facie case of obviousness under 35 U.S.C. §103(a).

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Additionally, Applicants re-assert that *Suzuki* and *Suga* are both directed solely to interlace scanning. Neither reference contains any disclosure, teaching, or suggestion regarding utilizing progressive mode and interlaced mode read-out in the same device. For at least this reason, Applicants submit that the Examiner's practice of equating frame-mode interlaced read-out as disclosed in *Suzuki* and *Suga* with the claimed progressive mode (full-frame in *Yamaguchi*) read-out is inaccurate and un-supported by the references. Furthermore, in light of the fact that *Yamaguchi* teaches away from interlaced scanning, Applicants submit that there can be no teaching or suggestion to combine the *Yamaguchi* with either one of the *Suzuki* or *Suga* references.

Accordingly, Applicants submit that claims 1 – 3 are allowable over the cited prior art, and respectfully request that the rejection be over-turned on appeal, and the remaining claims placed in condition for allowance. Additionally, because claims 4 – 6 inherit all of the limitations of the base claims 1 – 3, Applicants submit that the rejection of claims 4 – 6 must also be over-turned on appeal. In light of the forgoing, Applicants submit that this Application must be placed in condition for allowance.

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B. The Cited *Chang*, *Suzuki*, and *Suga* References Fail to Obviate the Claimed Invention as specified in Claims 1 – 6.

Applicants respectfully request reconsideration of the Examiner's rejection of claims 1 – 3 under 35 U.S.C. §103(a). Examiner has alternately rejected these claims in view of the cited prior art references of *Chang* (U.S. Patent No. 5,264,939), *Suzuki* (U.S. Patent No. 6,515,703), and *Suga* (U.S. Patent No. 4,963,980).

Under § 2143 of the MPEP, in order to establish a prima facie case of obviousness, the Examiner must meet three basic criteria. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." *MPEP §2143 rev. 3* (August, 2005). Applicants' assert that the Examiner has failed to establish a prima facie case of obviousness for at least the reasons that the prior art references fail to teach or suggest all of the claim limitations. Neither the primary reference nor any secondary reference provides any indication that two pre-determined bias voltages are applied to the substrate as a function of whether the imaging device is operating in progressive or interlaced field scanning mode, "so that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode."

Applicants note that the Examiner has conceded that the primary *Chang* reference fails to show any application of a bias voltage to the substrate of the image sensing portion that is smaller during progressive mode scan than during interlaced mod scan. (See page 13, second full paragraph of the May 16, 2006 Office Action). Additionally, the Examiner has

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conceded that neither the *Chang* nor the *Suzuki* reference show that the bias voltages are chosen such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced field mode. (See page 15, first partial paragraph of the May 16, 2006 Office Action).

The only issue Applicants wish to bring to the attention of the Board in regard to the *Chang* and *Suzuki* references is the proper distinction between progressive mode read-out and interlaced mode read-out. Progressive mode read-out is a method of reading-out charges stored in all of the image sensing devices in the imaging array at the same time, and wherein there is no mixing between adjacent photo-diodes. (See Column 2, lines 60 – 62 of *Suzuki*, which describes this mode and dismisses it as too costly compared to interlaced mode). Progressive mode read-out is disclosed, as cited by the Examiner, in Column 4, lines 38+ of the *Chang* reference.

In contrast to progressive mode, interlaced mode involves the read-out of less than all of the imaging devices in the imaging array at the same time. Interlaced mode has been implemented in two ways, frame-mode and field-mode. (Note that frame-mode is distinct from full-frame mode). In field mode interlaced scanning, adjacent pixels are read-out and mixed together in the vertical CCD register. (See Column 1, lines 36 – 40). In frame mode interlaced scanning, odd rows are read-out first, and then after the vertical CCD is done transferring the odd rows, the even row pixels are then read out.

Importantly, and counter to the Examiner's assertions throughout the last Office Action, the only reference cited by the Examiner that discloses a true progressive mode read-out is the *Chang* reference (directed to full-frame and thinning mode). Importantly, however, *Chang* fails to disclose, teach, or suggest a device capable of running in both interlaced mode

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and progressive mode, and actually teaches away from such a device. For example, *Chang* teaches the advantages of utilizing progressive mode read-out in Column 1, lines 55 – 65.

As clearly set forth in Column 4, lines 48 – 60, *Chang* does not disclose an imaging array capable of operating in both interlaced and progressive mode read-out. Rather, *Chang* discloses a method of summing and draining accomplished via registers 24, 26, and 28 (See Fig. 1 which effectively generate an interlaced signal for output. Importantly, however, even during the 'pseudo-interlaced output' mode, all pixels are read-out and transferred via the Vertical CCD just as in progressive mode. It is not until the image data is stored in the registers 24, 26, and 28 that further processing is executed in order to turn the progressive data into interlaced data. Accordingly, Chang fails to meet the claim limitations requiring a photoelectric conversion portion capable of reading-out picture elements in progressive mode and in interlaced mode. Additionally, one of ordinary skill in the art would not be motivated to combine either of the *Suzuki* or *Suga* references with *Chang*, as *Chang* reads out the signals from the individual pixels in a progressive mode no matter whether the eventual signal output is progressive or interlaced. Accordingly, application of varying substrate voltages from *Suzuki* and/or *Suga* is not possible with Chang, as Chang only allows for progressive mode read-out of the individual pixels.

The two other references cited by the Examiner, *Suzuki* and *Suga*, are both directed solely to interlace scanning. There is no disclosure at all in either of these references to progressive mode read-out, absent the casual mention in Column 2, line 67 – Column 3, line 2 of *Suzuki* that progressive mode read-out is too expensive and is not generally used. While the remaining references do compare field-mode interlaced scanning in which adjacent pixels are mixed in the Vertical CCD to frame-mode interlaced scanning in which only the odd

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pixels are read-out and transferred (un-mixed) before the even pixels are read-out and transferred (unmixed), neither reference contains any disclosure, teaching, or suggestion regarding utilizing progressive mode and interlaced mode read-out in the same device. For at least this reason, Applicants submit that the Examiner's practice of equating frame-mode interlaced read-out as disclosed in *Suzuki* and *Suga* with the claimed progressive mode read-out is inaccurate and un-supported by the references.

Furthermore, in light of the fact that *Chen* teaches away from interlaced read-out of the individual pixels, Applicants submit that there can be no teaching or suggestion to combine the *Chen* reference with either one of the *Suzuki* or *Suga* references.

Applicants submit that, for at least these reasons, the Examiner's rejection cannot be sustained and should be reversed on Appeal.

Absent the above contention regarding the cited prior art references, the single remaining contention between Applicants and the Examiner is whether the *Suga* reference discloses the limitation wherein two pre-determined bias voltages are applied to the substrate as a function of whether the imaging device is operating in progressive or interlaced field scanning mode, "so that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode."

Applicants will not proceed to make the same arguments set forth in regard to the Examiner's rejection of the claims under *Yamaguchi*. Rather, Applicants re-iterate and respectfully direct the Board's attention to the arguments set forth above regarding the *Suga* reference. Specifically, Applicants submit that the Examiner has failed to cite any portion of the *Suga* reference which anticipates the claim limitation requiring that the saturation signal quantities are substantially equivalent in both interlaced (mixing) and progressive (no-

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mixing), and that the Examiner has thus failed to assert a prima facie case of obviousness under 35 U.S.C. §103(a).

Additionally, Applicants re-assert that *Suzuki* and *Suga* are both directed solely to interlace scanning. Neither reference contains any disclosure, teaching, or suggestion regarding utilizing progressive mode and interlaced mode read-out in the same device. For at least this reason, Applicants submit that the Examiner's practice of equating frame-mode interlaced read-out as disclosed in *Suzuki* and *Suga* with the claimed progressive mode read-out is inaccurate and un-supported by the references. Furthermore, in light of the fact that *Chen* teaches away from interlaced scanning, Applicants submit that there can be no teaching or suggestion to combine the *Chen* with either one of the *Suzuki* or *Suga* references.

Accordingly, Applicants submit that claims 1 – 3 are allowable over the cited prior art, and respectfully request that the rejection be over-turned on appeal, and the remaining claims placed in condition for allowance. Additionally, because claims 4 – 6 inherit all of the limitations of the base claims 1 – 3, Applicants submit that the rejection of claims 4 – 6 must also be over-turned on appeal. In light of the forgoing, Applicants submit that this Application must be placed in condition for allowance.

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CONCLUSION

In light of the foregoing, Applicant submits that the rejections of all claims are improper for the reasons noted and the rejections should all therefore be withdrawn.

Respectfully submitted,

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(Reg. #37,607)

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VIII. CLAIMS APPENDIX:

This listing of claims reflects the current status of the claims as they stand in light of the August 4, 2005 Final Office Action:

1. (Rejected) A solid-state image sensor device having an image sensing portion performing photoelectric conversion in both progressive mode in which all picture element signals are output independently, and interlaced mode in which interlaced scannings are performed and the picture element signals obtained in respective scannings in said image sensing portion are superimposed, said sensor device comprising:

a photodiode within the image sensing portion; and

a substrate-bias generation circuit for applying a bias voltage to the substrate of said image sensing portion and for controlling said bias voltage in said progressive mode to be smaller than the bias voltage while operating in the interlaced mode; and

wherein the applied bias voltages are chosen such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode.

2. (Rejected) A driving method for a solid-state image sensor device having an image sensing portion including a photodiode within the image sensing portion for performing photoelectric conversion said image sensing portion operating in both progressive mode in which all picture element signals are output independently, and interlaced mode in which a plurality of scannings are performed and picture element signals obtained in respective scannings are superimposed, said method including applying a bias voltage to the substrate of said image sensing portion, wherein during said progressive mode said bias

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voltage is smaller than that in said interlaced mode; and wherein the applied bias voltages are chosen such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode.

3. (Rejected) A camera comprised of a solid-state image sensor device having an image sensing portion for performing photoelectric conversion and a substrate-bias generation circuit, an optical system receiving incident light from a subject and forming an image on said image sensing portion of said solid-state image sensor device, a driving system for driving said solid-state image sensor device, and a signal processing system for processing the signal output from said solid-state image sensor device to obtain a video signal, wherein the image sensing portion includes a photodiode structure, and further

wherein said driving system selectively operates in progressive mode in which all picture element signals are output independently, and interlaced mode in which a plurality of scannings are performed and the picture element signals obtained in respective scannings are superimpose, and wherein the bias voltage applied to the substrate in said progressive mode is smaller than that in said interlaced mode; and

wherein the applied bias voltages are chosen such that a saturation signal quantity in the progressive mode is substantially equivalent to that in the interlaced mode.

4. (Rejected) The solid state image sensor device of claim 1, wherein the substrate bias generation circuit adjusts the substrate bias voltage during the progressive mode of operation such that a potential difference is generated between a doped region and a

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well of the photodiode which is greater than during interlaced operation and further wherein the photodiode is a hole accumulation diode.

5. (Rejected) The method of driving a solid state image sensor device of claim 2, wherein the step of applying the substrate bias voltage during the progressive mode of operation is performed such that a potential difference is generated between a doped region and a well of the photodiode which is greater than during interlaced operation and further wherein the photodiode is a hole accumulation diode.

6. (Rejected) The camera of claim 3, further comprising: applying the substrate bias voltage during the progressive mode of operation such that a potential difference is generated between a doped region and a well of the photodiode which is greater than during interlaced operation and further wherein the photodiode is a hole accumulation diode.

Claims 7 - 18. (Canceled).

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IX. EVIDENCE APPENDIX:

None.

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X. RELATED PROCEEDINGS APPENDIX:

None.

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